IN THE CLAIMS:

Please substitute the following claims for the same-numbered claims in the application.

1. (Currently Amended) A liquid crystal display, comprising:

liquid crystal cells forming an image display area on a substrate; and

a driver for applying a voltage to said liquid crystal cells based on a reference voltage for gamma correction corresponding to digital input data, wherein said driver keeps a number of switching times for pulse strings per time unit constant for a predetermined range of said digital input data when generating the pulse strings with pulse densities corresponding to said digital input data, wherein said pulse strings comprise a frequency characteristic having a trapezoidal shape corresponding to said digital input data[[.]], wherein said driver comprises a pulse generation circuit for generating a plurality of reference pulses in which pulse generation densities are weighted; and a pulse select/synthesis circuit for generating a pulse string by selecting and synthesizing necessary reference pulses on the basis of digital input data and reference pulses, and wherein said pulse select/synthesis circuit outputs a logical sum between a carry output from an adder circuit, which has as its inputs high order W bits of the digital input data of n bits and low order W bits of a binary counter, and a logical product between outputs X(m-1) through X(0) of said pulse generation circuit where m=n-W and the digital input data D(m-1) through D(0).

2. (Original) The liquid crystal display according to claim 1, wherein said driver is formed on said substrate and is comprised of a plurality of driver ICs connected via signal lines.

3. (Original) The liquid crystal display according to claim 1, wherein said predeter... range of said digital input data is a predetermined range around a medium value of said... input data.

4. (Currently Amended) A liquid crystal display, comprising:

liquid crystal cells forming an image display area on a substrate; and

a driver for applying a voltage to said liquid crystal cells based on a reference v... gamma correction corresponding to digital input data, wherein said driver has no local p... number of switching times for pulse strings per time unit when generating the pulse strings with pulse densities corresponding to said digital input data, wherein said pulse strings comprise ... frequency characteristic having a trapezoidal shape corresponding to said digital input da..., wherein said driver comprises a pulse generation circuit for generating a plurality of ref... pulses in which pulse generation densities are weighted; and a pulse select/synthesis cir... generating a pulse string by selecting and synthesizing necessary reference pulses on the... digital input data and said reference pulses, and wherein said pulse select/synthesis circu... outputs a logical sum between a carry output from an adder circuit, which has as its inputs... order W bits of the digital input data of n bits and low order W bits of a binary counter, an... logical product between outputs X(m-1) through X(0) of said pulse generation circuit wh... m=n-W and the digital input data D(m-1) through D(0).

5. (Currently Amended) A liquid crystal display, comprising:

liquid crystal cells forming an image display area on a substrate; and

a driver for applying a voltage to said liquid crystal cells based on a reference voltage for gamma correction corresponding to digital input data, wherein said driver obtains an output voltage using pulse density modulation (PDM) as well as obtains an output voltage using pulse width modulation (PWM) for a predetermined range of said digital input data around a transition value when generating pulse strings corresponding to said digital input data, wherein said pulse strings comprise a frequency characteristic having a trapezoidal shape corresponding to said digital input data[[.]], wherein said driver comprises a pulse generation circuit for generating a plurality of reference pulses in which pulse generation densities are weighted; and a pulse select/synthesis circuit for generating a pulse string by selecting and synthesizing necessary reference pulses on the basis of digital input data and said reference pulses, and wherein said pulse select/synthesis circuit outputs a logical sum between a carry output from an adder circuit which has as its inputs high order W bits of the digital input data of n bits and low order W bits of a binary counter, and a logical product between outputs X(m-1) through X(0) of said pulse generation circuit where m=n-W and the digital input data D(m-1) through D(0).

6. (Currently Amended) A liquid crystal display driver for applying a voltage to liquid crystal cells forming an image display area, comprising:

a pulse generation circuit for generating a plurality of reference pulses in which pulse generation densities are weighted; ~~and~~

a pulse select/synthesis circuit for generating a pulse string by selecting and synthesizing necessary reference pulses on the basis of digital input data and said reference pulses, wherein

said pulse generation circuit generates said reference pulses without changing a number of switching times per time unit for a predetermined range of said digital input data around a medium value, wherein said pulse strings comprise a frequency characteristic having a trapezoidal shape corresponding to said digital input data[[.]]; and

an integration circuit for integrating the pulse string generated by said pulse select/synthesis circuit to output a voltage for gamma correction,

wherein said pulse select/synthesis circuit outputs a logical sum between a carry from an adder circuit, which has as its inputs high order W bits of the digital input data and low order W bits of a binary counter, and a logical product between outputs X(m-1) ... X(0) of said pulse generation circuit where m=n-W and the digital input data D(m-1) thru D(0).

7. (Cancelled).

8. (Cancelled).

9. (Currently Amended) The liquid crystal display driver according to claim [[7]] 6, assuming that said digital input data is n bits, wherein said pulse generation circuit outputs reference pulses using an n-bit binary counter, an n-1 bit latch, and n-1 2-input gates.

10. (Previously Presented) A reference pulse generation circuit for generating reference pulses corresponding to n-bit digital input data, comprising:

an n-bit binary counter for counting up in synchronization with an input clock;

an n-1 bit latch for generating signals by delaying high order n-1 bits output B(n-1) through B(1) from said binary counter by one input clock period; and

n-1 logical circuits for performing logical operations with receiving as inputs said high order n-1 bits output B(n-1) through B(1) from said binary counter and the delayed signals corresponding to the high order n-1 bits output B(n-1) through B(1) from said n-1 bit latch, obtaining outputs X(0) through X(n-2) with lower reference pulse densities, whereas output X(n-1) is obtained bypassing the logical circuit, wherein said reference pulses comprise a frequency characteristic having a trapezoidal shape corresponding to said n-bit digital input data.

11. (Original) The reference pulse generation circuit according to claim 10, wherein said n-1 logical circuits are n-1 AND circuits.

12. (Original) The reference pulse generation circuit according to claim 10, wherein said n-1 logical circuits are n-2 AND circuits outputting X(0) through X(n-3) and a NOR circuit outputting X(n-2).

13. (Currently Amended) A reference pulse generation circuit for digital-analog conversion employing a pulse density modulation scheme, comprising:

means for generating reference pulses that are exclusively in a high state corresponding to digital input data; and

means for generating the reference pulses such that a number of switching times

strings per time unit is constant for a predetermined range of said digital input data around a medium value, wherein said pulse strings comprise a frequency characteristic having a trapezoidal shape corresponding to said digital input data[[.]], wherein said reference pulses comprise pulse generation densities that are weighted, and wherein said pulse strings are generated by selecting and synthesizing necessary reference pulses on the basis of digital data and said reference pulses;

means for integrating the pulse strings to output a voltage for gamma correction; and

means for outputting a logical sum between a carry output from an adder circuit that has as its inputs high order W bits of the digital input data of n bits and low order W bits of a binary counter, and a logical product between outputs X(m-1) through X(0) of said pulse generation circuit where m=n-W and the digital input data D(m-1) through D(0).

14. (Original) The reference pulse generation circuit according to claim 13, wherein the reference pulses are generated with the frequency thereof being kept constant for half the range of said digital input data.

15. (Currently Amended) A method for generating reference pulses in a digital-analog converter, said method comprising:

generating pulse strings with pulse densities corresponding to digital input data for input to said digital-analog converter; and

keeping a number of switching times for said pulse strings per time unit constant for a predetermined range of said digital input data around a medium value, wherein said pulse strings

comprise a frequency characteristic having a trapezoidal shape corresponding to said digital input data, wherein said reference pulses comprise pulse generation densities that are weighted, and wherein said pulse strings are generated by selecting and synthesizing necessary reference pulses on the basis of digital input data and said reference pulses;

integrating the pulse strings to output a voltage for gamma correction; and

outputting a logical sum between a carry output from an adder circuit, which has as its inputs high order W bits of the digital input data of n bits and low order W bits of a bit counter, and a logical product between outputs X(m-1) through X(0) of said pulse generation circuit where m=n-W and the digital input data D(m-1) through D(0).

16. (Original) The method according to claim 15, further comprises the step of reducing the maximum frequency of said pulse strings to less than half of that in the case where the switching times is not kept constant.

17. (Currently Amended) A method for providing an analog voltage output corresponding to digital input data, said method comprising:

generating reference pulses that are exclusively in a high state corresponding to digital input data;

for a range of said digital input data excluding a predetermined range around a medium value, integrating a pulse string, whose number of pulses is adjusted depending on said digital input data, to output an analog voltage; and

for the predetermined range of said digital input data around said medium value,

integrating a pulse string, whose duty is adjusted depending on said digital input data, to an analog voltage, wherein said pulse strings comprise a frequency characteristic having a trapezoidal shape corresponding to said digital input data wherein said reference pulses have pulse generation densities that are weighted, and wherein said pulse strings are generated by selecting and synthesizing necessary reference pulses on the basis of digital input data and said reference pulses;

integrating the pulse string to output a voltage for gamma correction; and

outputting a logical sum between a carry output from an adder circuit, which has as its inputs high order W bits of the digital input data of n bits and low order W bits of a binary counter, and a logical product between outputs X(m-1) through X(0) of said pulse generation circuit where m=n-W and the digital input data D(m-1) through D(0).

18. (Original) The method according to claim 17, further comprises the step of using said output analog voltage for a reference voltage for gamma correction in a source driver of a liquid crystal display.

19. (Previously Presented) A liquid crystal display driver for applying a voltage to liquid crystal cells forming an image display area, comprising:

a pulse generation circuit for generating a plurality of reference pulses in which pulse generation densities are weighted;

a pulse select/synthesis circuit for generating a pulse string by selecting and synthesizing necessary reference pulses on the basis of digital input data and said reference pulses, which are

said pulse generation circuit generates said reference pulses without changing a number of switching times per time unit for a predetermined range of said digital input data around a medium value, wherein said pulse strings comprise a frequency characteristic having a trapezoidal shape corresponding to said digital input data;

an integration circuit for integrating the pulse string generated by said pulse select/synthesis circuit to output a voltage for gamma correction,

wherein said pulse select/synthesis circuit outputs a logical sum between a carry-out from an adder circuit, which has as its inputs high order W bits of the digital input data D(m-1) through D(n) and low order W bits of a binary counter, and a logical product between outputs X(m-1) through X(0) of said pulse generation circuit where m=n-W and the digital input data D(m-1) through D(0), and

wherein if said digital input data is n bits, then said pulse generation circuit outputs reference pulses using an n-bit binary counter, an n-1 bit latch, and n-1 2-input gates.

20. (Previously Presented) A reference pulse generation circuit for generating reference pulses corresponding to n-bit digital input data, consisting of:

an n-bit binary counter for counting up in synchronization with an input clock;

an n-1 bit latch for generating signals by delaying high order n-1 bits output B(n-1) through B(1) from said binary counter by one input clock period; and

n-1 logical circuits for performing logical operations with receiving as inputs said high order n-1 bits output B(n-1) through B(1) from said binary counter and the delayed signals corresponding to the high order n-1 bits output B(n-1) through B(1) from said n-1 bit latch and

obtaining outputs X(0) through X(n-2) with lower reference pulse densities, whereas output X(n-1) is obtained bypassing the logical circuit, wherein said reference pulses comprise a frequency characteristic having a trapezoidal shape corresponding to said n-bit digital input data,

wherein said n-1 logical circuits are n-1 AND circuits, and

wherein said n-1 logical circuits are n-2 AND circuits outputting X(0) through X(n-3), and a NOR circuit outputting X(n-2).

This Page is Inserted by IFW Indexing and Scanning Operations and is not part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☐ BLACK BORDERS
- ☐ IMAGE CUT OFF AT TOP, BOTTOM OR SIDES
- ☐ FADED TEXT OR DRAWING
- ☐ BLURRED OR ILLEGIBLE TEXT OR DRAWING
- ☐ SKEWED/SLANTED IMAGES
- ☐ COLOR OR BLACK AND WHITE PHOTOGRAPHS
- ☐ GRAY SCALE DOCUMENTS
- ☒ LINES OR MARKS ON ORIGINAL DOCUMENT
- ☐ REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY
- ☐ OTHER: _____

IMAGES ARE BEST AVAILABLE COPY.
As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.